FIG. 1
Al BOND PAD

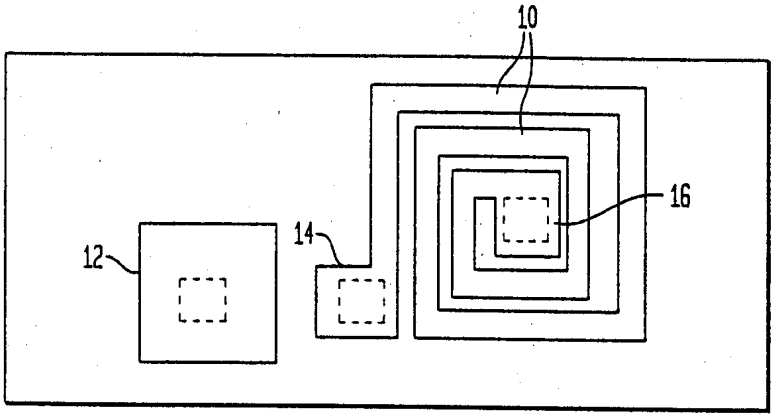

FIG. 1A
LAST METAL Cu FORMATION

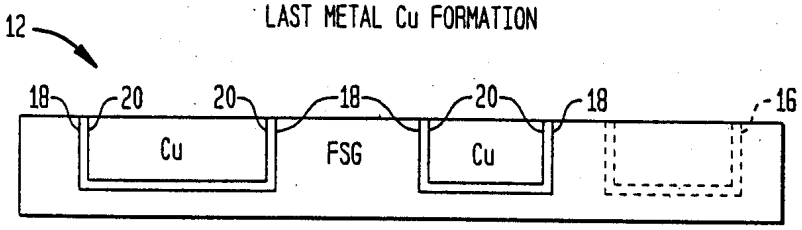

FIG. 1B
SiN/SiO2/SiN PASSIVATION DEPOSITION

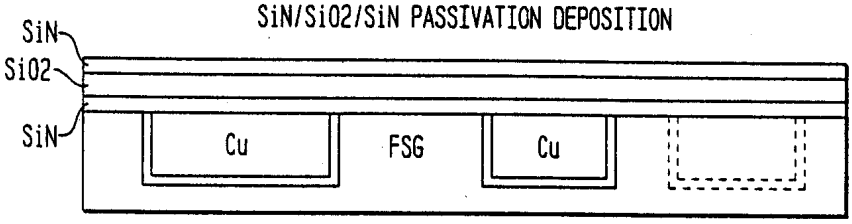

FIG. 1C
TERMINAL VIA PATTERNING

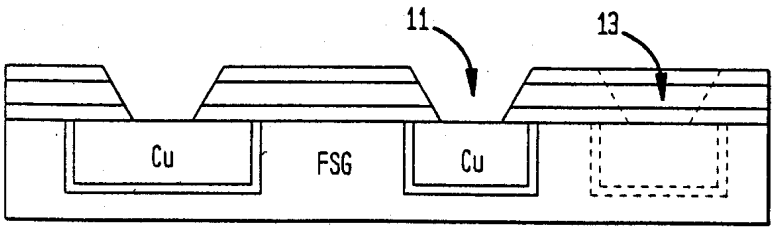

FIG. 1D
PATTERN Al BOND PAD, TaN BARRIER, Cu SEED

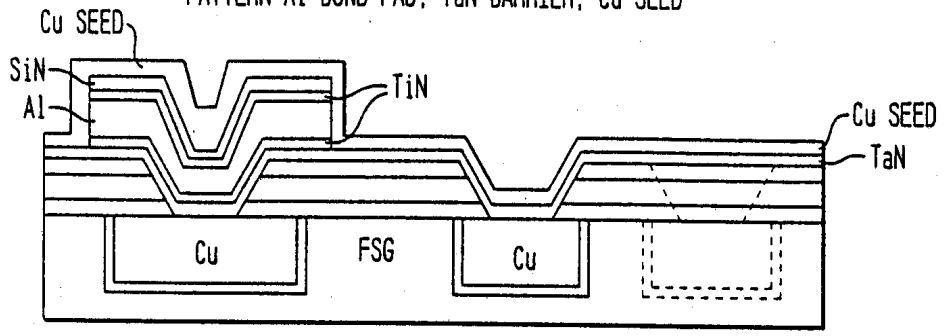

FIG. 1E
RESIST PATTERN AND Cu PLATING FOR INDUCTOR

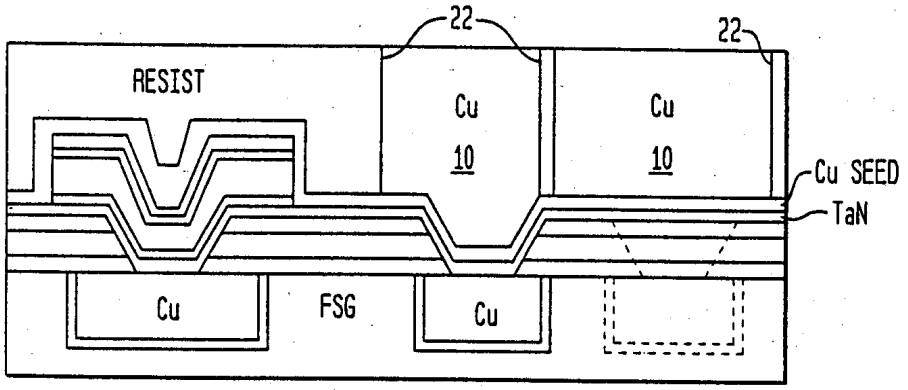

FIG. 1F
RESIST STRIP, Cu ETCH, TaN ETCH, CoWP SELECTIVE DEP.

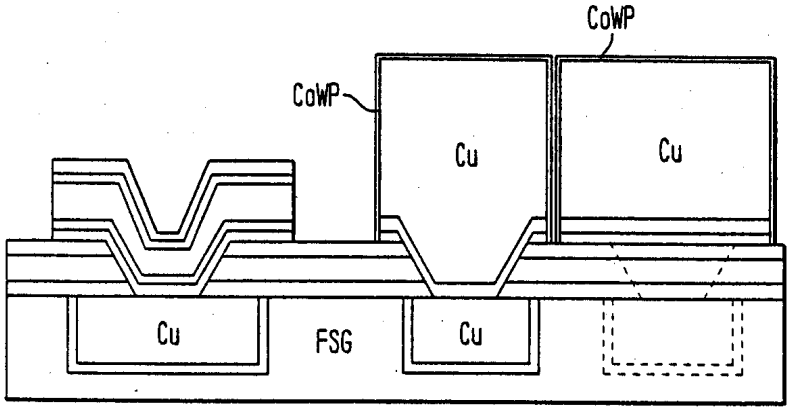

FIG. 1G
POLYMIDE APPLY, FINAL VIA OPENING

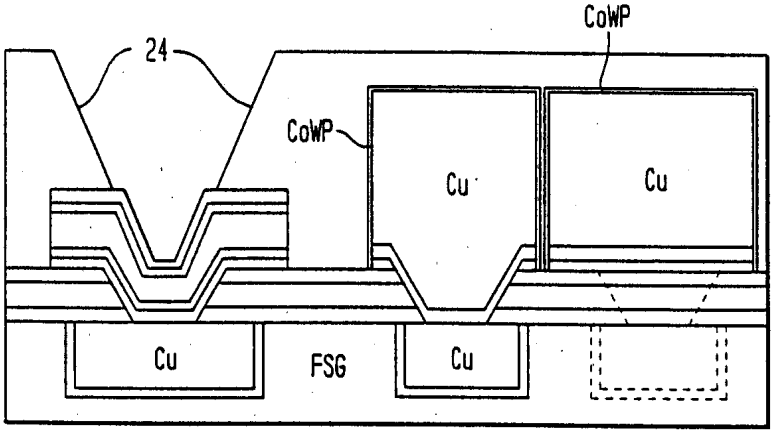

FIG. 1H
ETCH SiN, DEP. BARRIER, FORM C4 SOLDER BUMPS

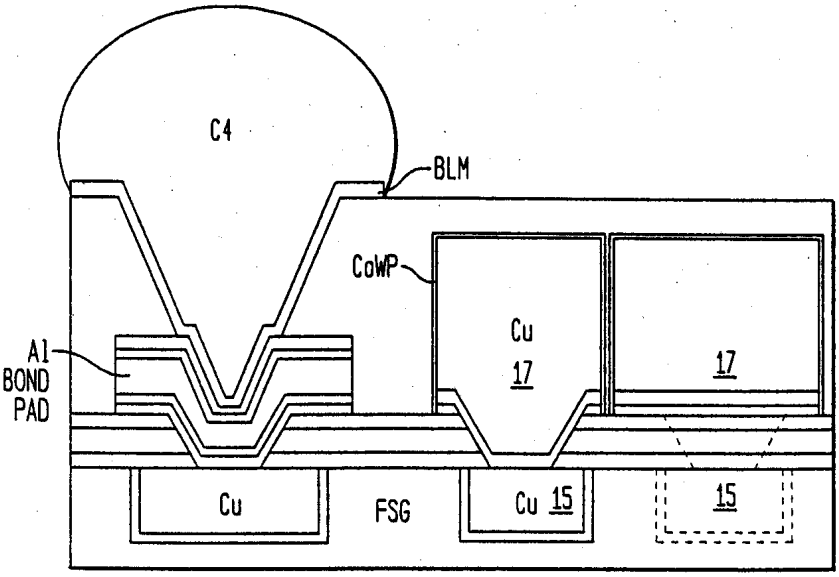

FIG. 2
Cu BOND PAD

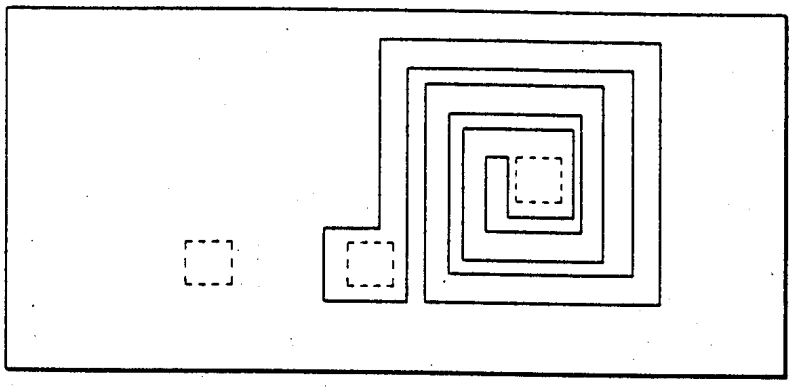

FIG. 2D
DEPOSIT TaN BARRIER

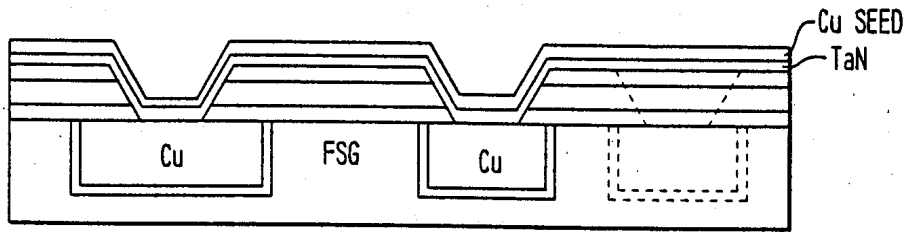

FIG. 2E
RESIST PATTERN AND Cu PLATING FOR INDUCTOR

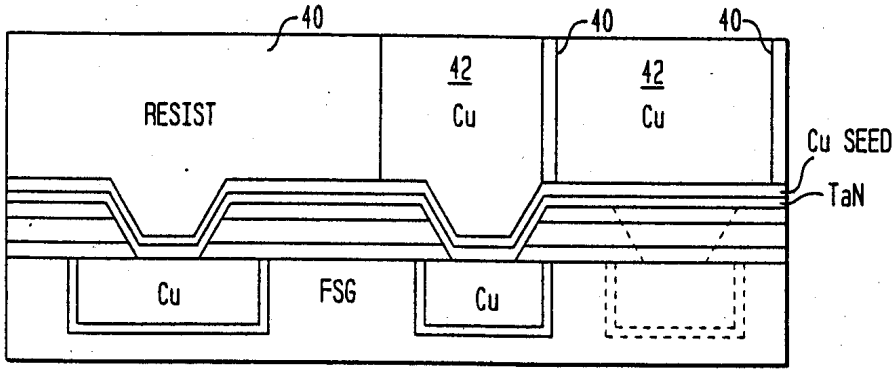

FIG. 2F
RESIST STRIP, Cu ETCH, TaN ETCH, CoWP SELECTIVE DEP.

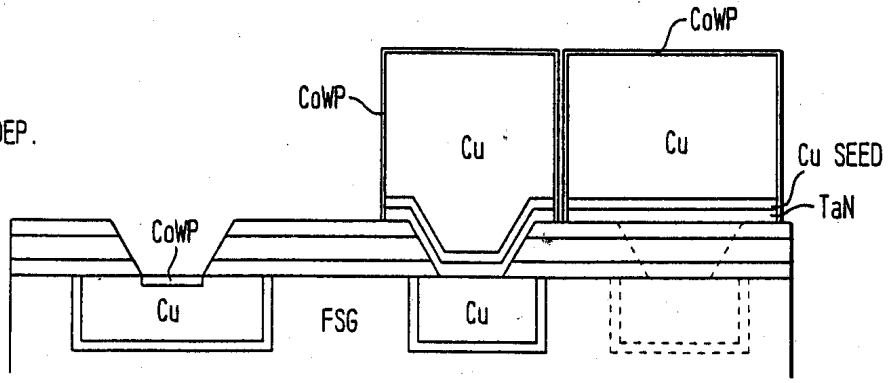

FIG. 2G
POLYIMIDE APPLY, FINAL VIA OPENING

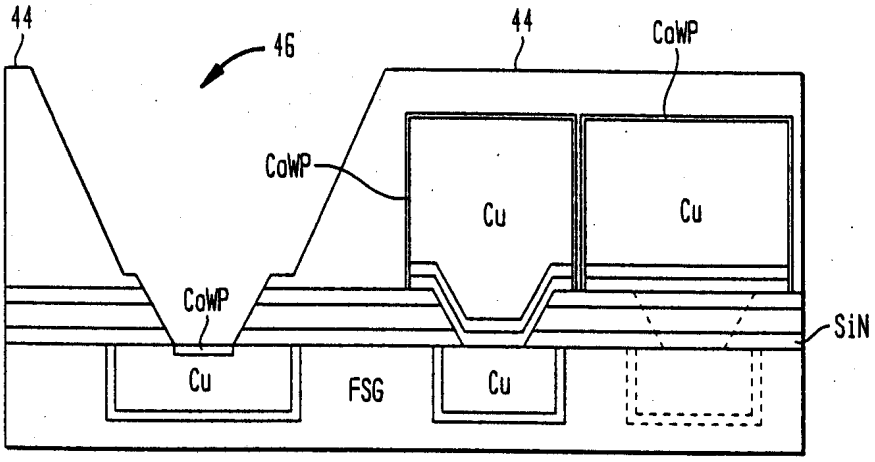

FIG. 2H
ETCH SiN, DEP. BARRIER, FORM C4 SOLDER BUMPS

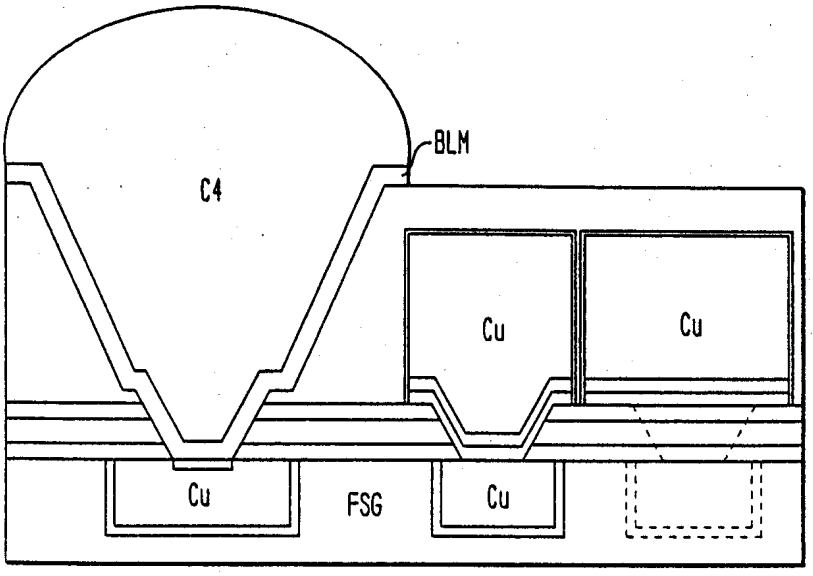

FIG. 3
RAISED Cu BOND PAD

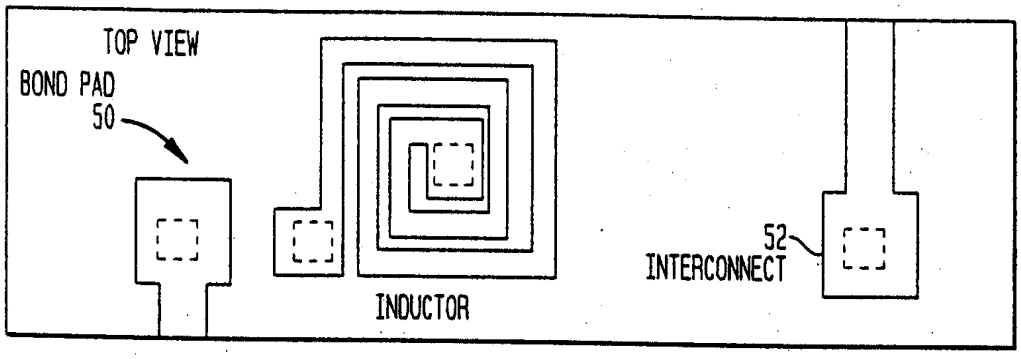

FIG. 3E
RESIST PATTERN AND Cu PLATING FOR INDUCTOR

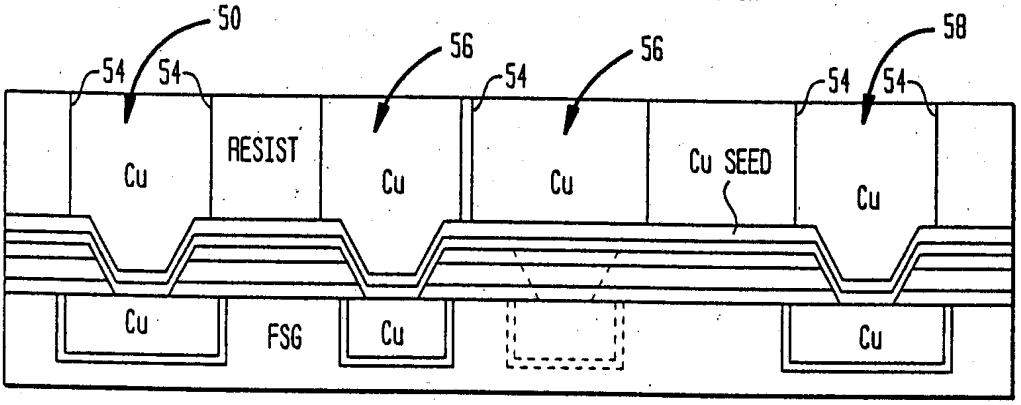

FIG. 3F
RESIST STRIP, TaN ETCH, CoWP SELECTIVE DEP.

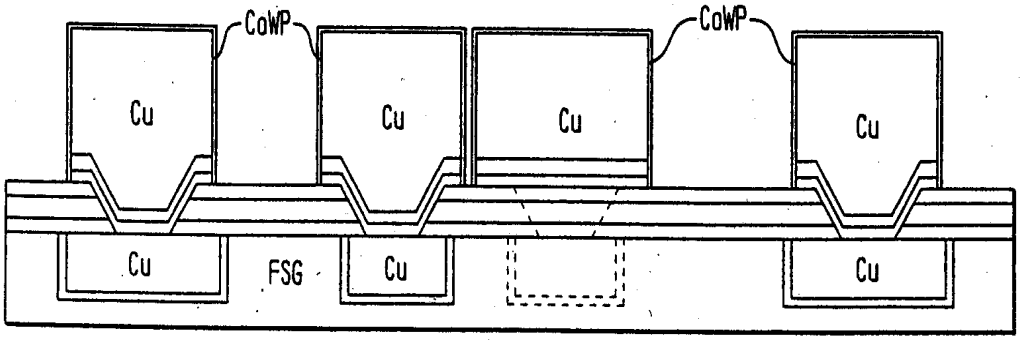

FIG. 3G
POLYIMIDE APPLY, FINAL VIA OPENING

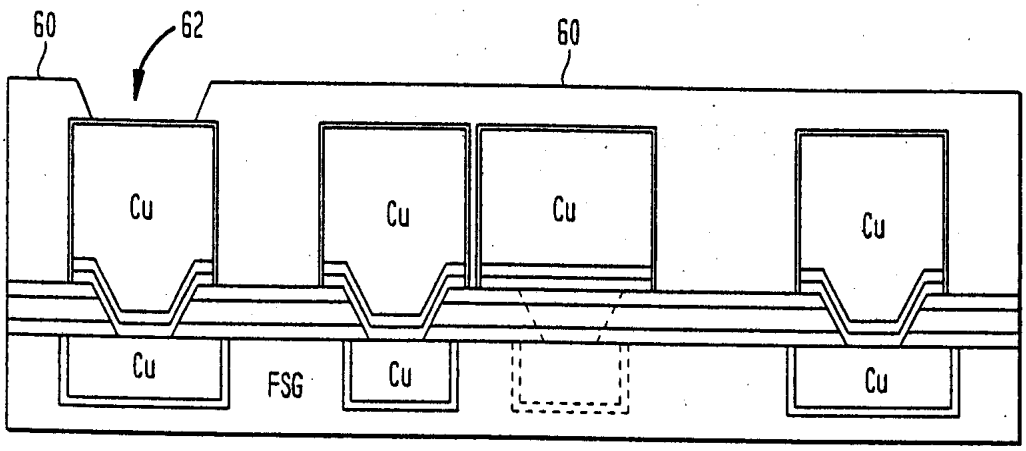

FIG. 3H
ETCH SiN, DEP. BARRIER, FORM C4 SOLDER BUMPS

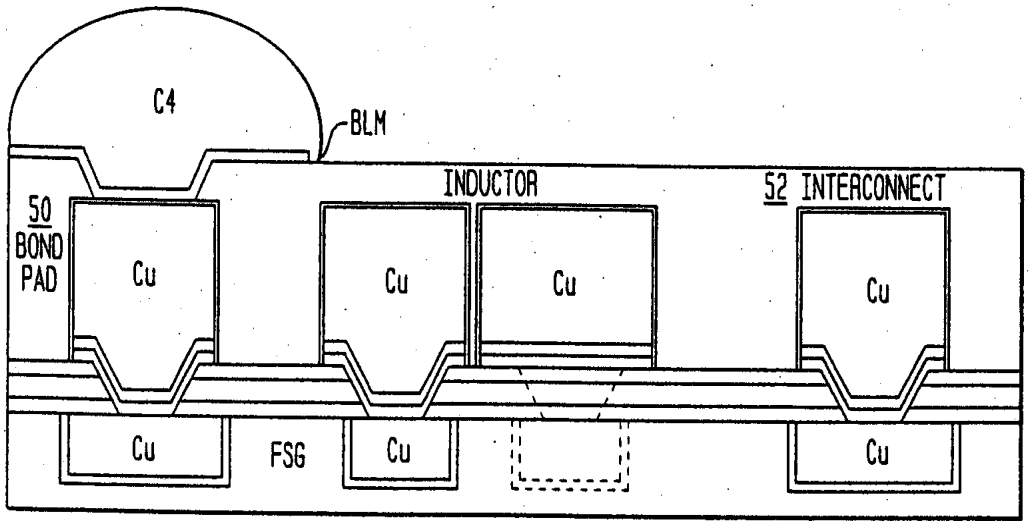

FIG. 4A
DEPOSIT TaN BARRIER AND Cu SEED

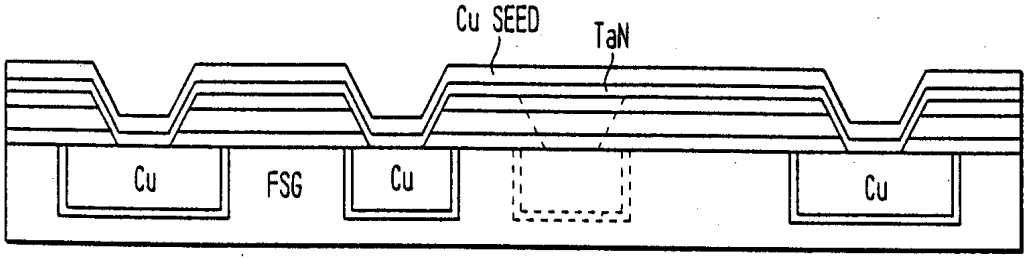

FIG. 4B
RESIST PATTERN AND SELECTIVE Cu PLATING FOR INDUCTOR

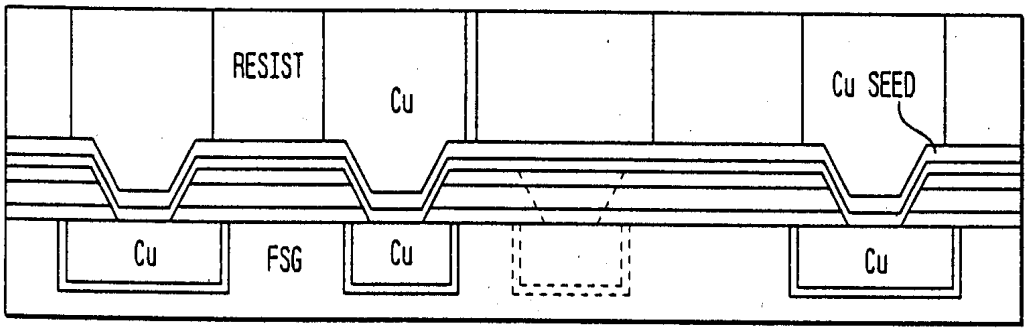

FIG. 4C
STRIP RESIST; ETCH Cu SEED AND BARRIER

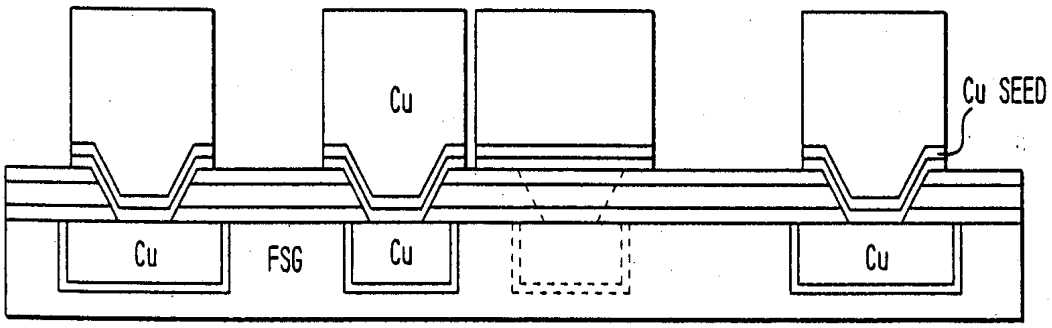

FIG. 5A
DEPOSIT TaN BARRIER

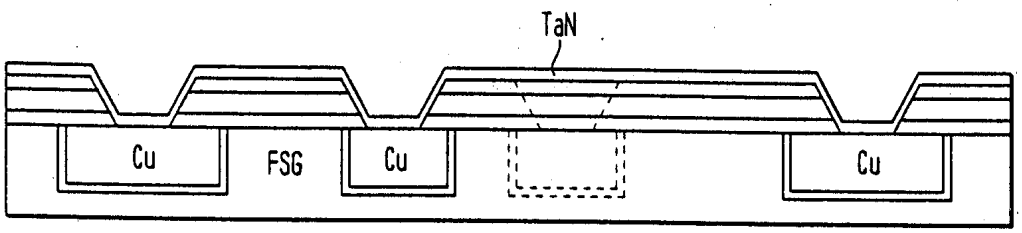

FIG. 5B
RESIST PATTERN; DEPOSIT ADHESION LAYER AND Cu SEED

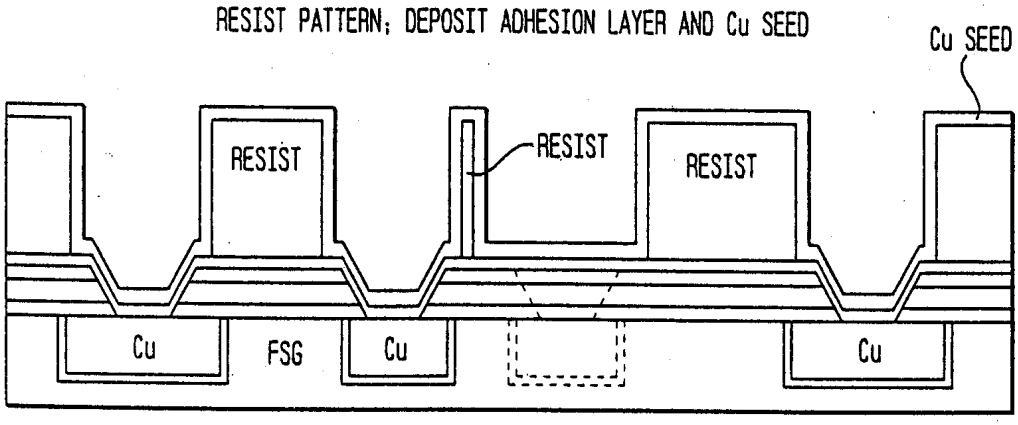

FIG. 5C
Cu PLATING

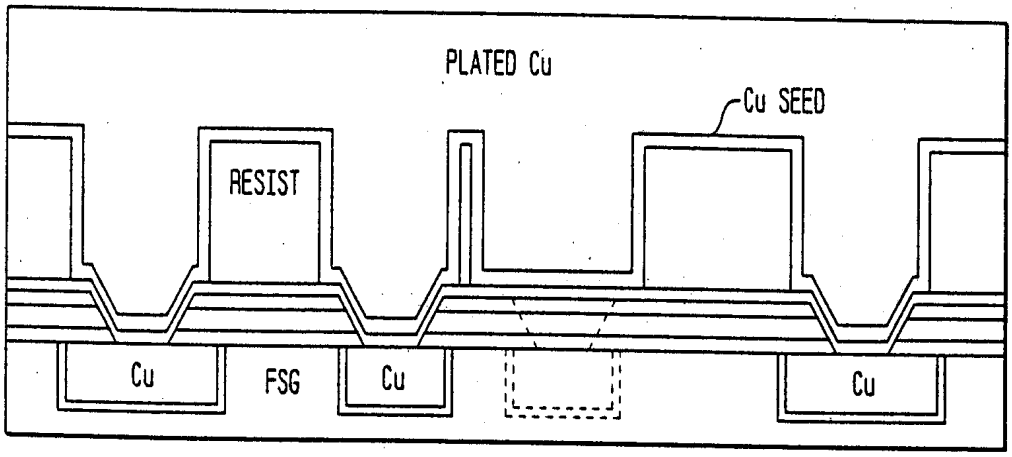

FIG. 5D
Cu CMP OR ELECTROPLATING

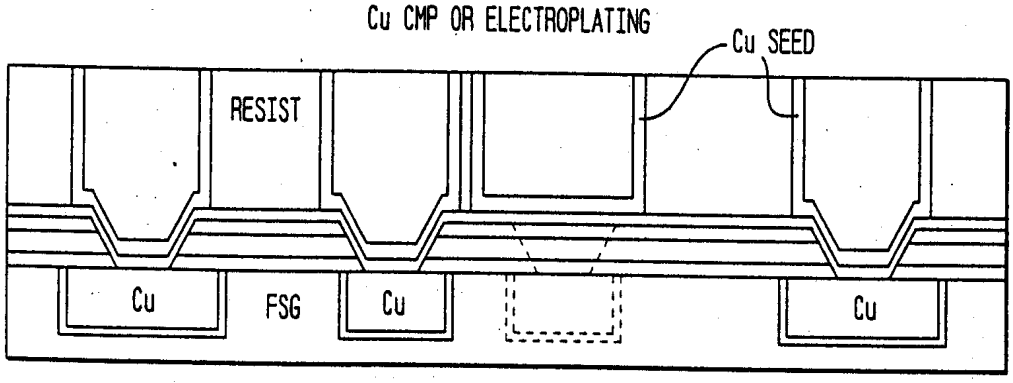

FIG. 5E
RESIST STRIP AND BARRIER ETCH

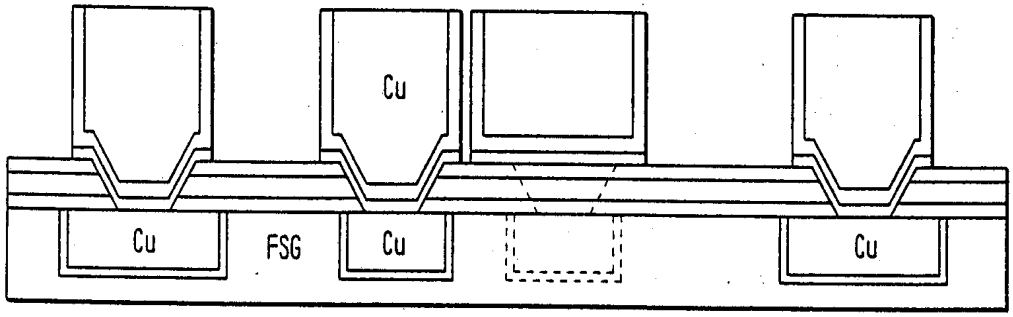

FIG. 6A
TERMINAL VIA PATTERNING

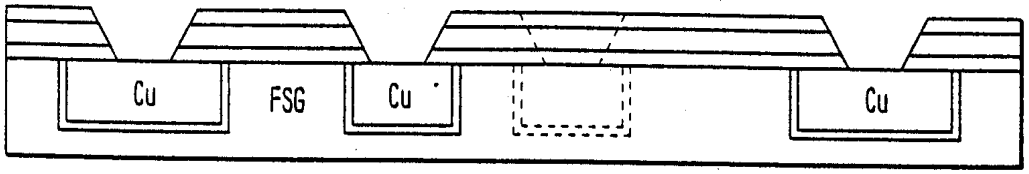

FIG. 6B
RESIST PATTERN; TaN AND Cu SEED

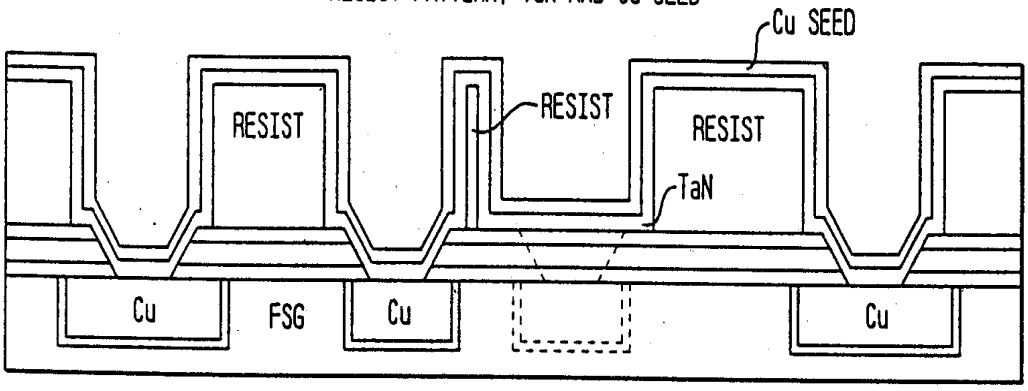

FIG. 6C
Cu PLATING

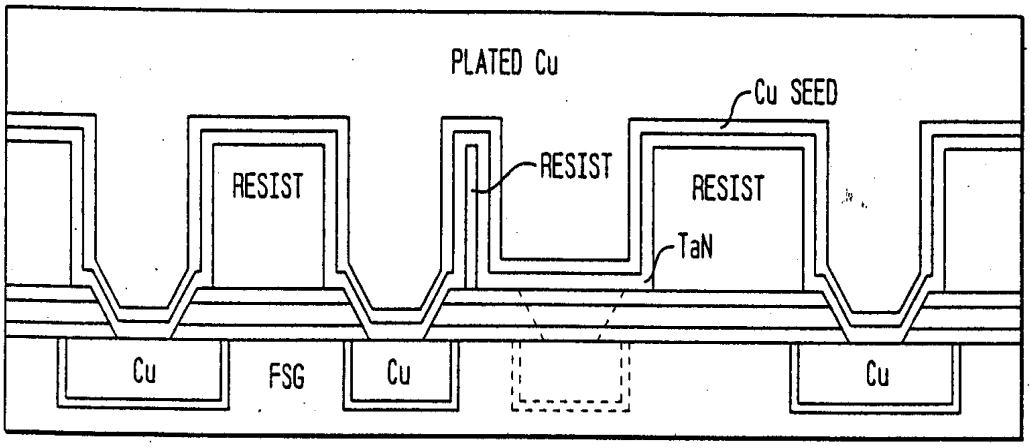

FIG. 6D
Cu CMP OR ELECTROPLATING, TaN, CMP OR RIE

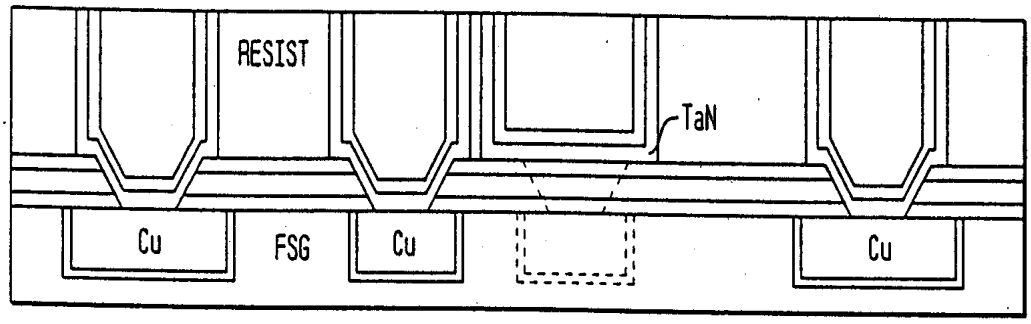

FIG. 6E
RESIST STRIP

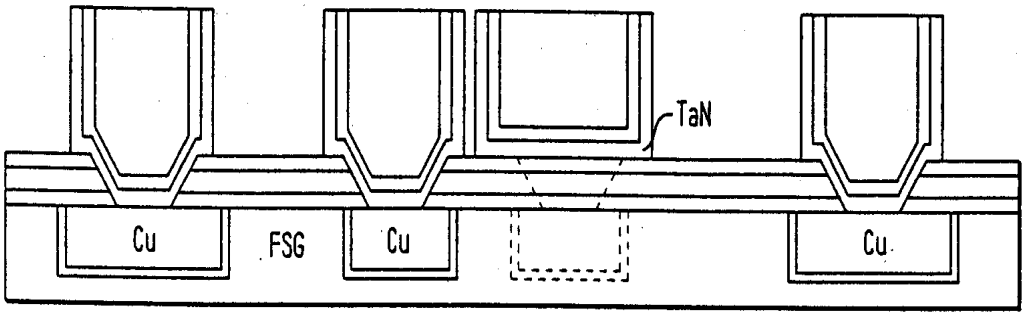

FIG. 7A
SELECTIVE METAL ONLY

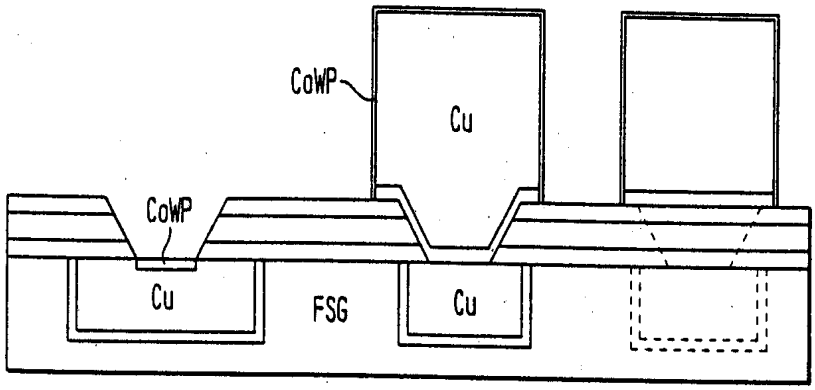

FIG. 7B
DIELECTRIC DEPOSITION ONLY (SINGLE LAYER OR MULTILAYER)

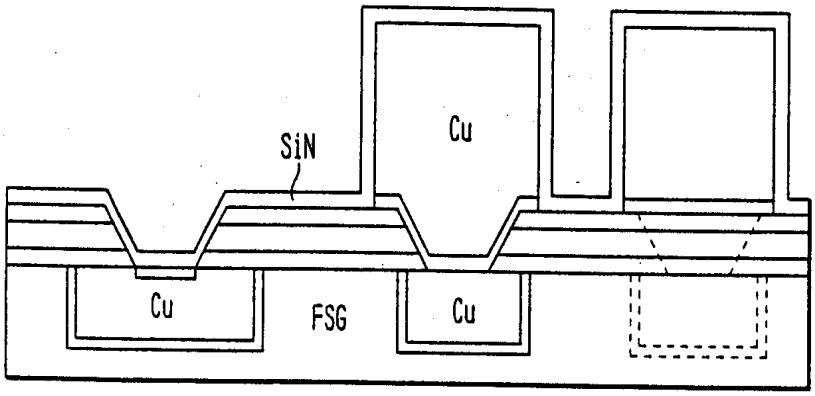

FIG. 7C
SELECTIVE METAL AND DIELECTRIC

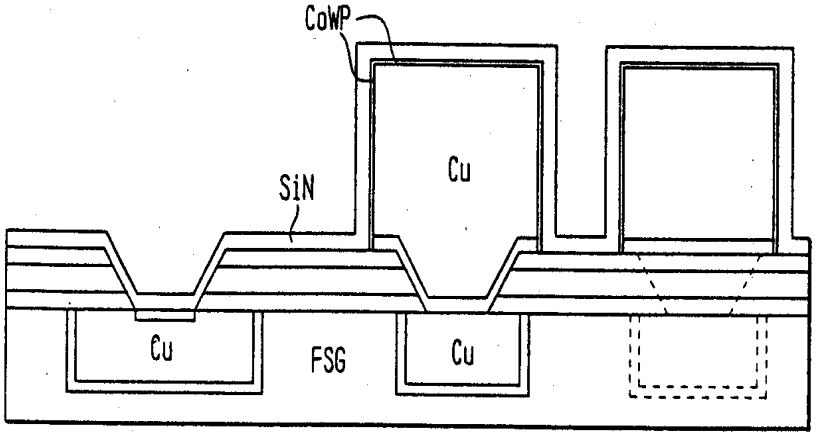

FIG. 7D
SPACER (METAL OR INSULATOR) AND DIELECTRIC DEPOSITION

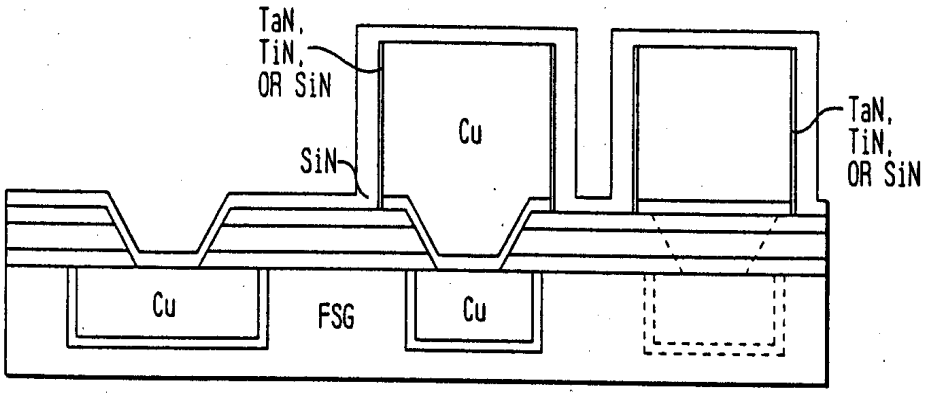

FIG. 7E
SPACER (METAL OR INSULATOR) AND
SELECTIVE METAL AND DIELECTRIC DEPOSITION

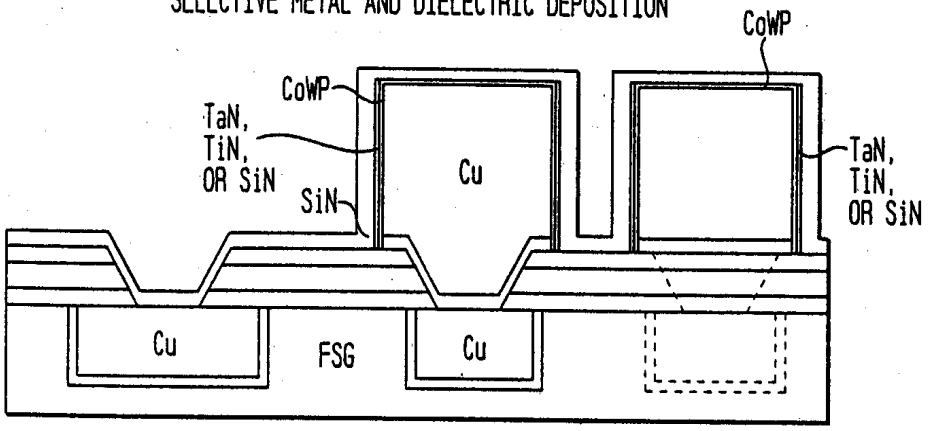

FIG. 7F
SELECTIVE METAL AND SPACER
(METAL OR INSULATOR) AND DIELECTRIC DEPOSITION